

REMARKS

Favorable consideration and allowance of the claims of the present application are respectfully requested.

Before addressing the specific grounds of rejection raised in the outstanding Office Action, applicants have amended Claims 1, 2 and 8 to positively recite that the claimed resistor is a *metal* resistor. Support for this amendment to Claims 1, 2 and 8 is found throughout the originally filed application. See, for example, paragraphs [0001] and [0021].

Since the above amendment to the claims does not introduce any new matter into the originally filed application, entry thereof is respectfully requested.

In the outstanding Office Action, Claims 1-3, 5-8 and 10 stand rejected under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. Patent No. 6,586,311 to Wu ("Wu"). Claim 4 stands rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Wu and U.S. Patent No. 6,777,752 to Osanai et al. ("Osanai et al."). Claim 9 stands rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Wu and U.S. Patent No. 5,554,873 to Erdeljac et al. ("Erdeljac et al.").

Concerning the § 102(b) rejection, it is axiomatic that anticipation under § 102 requires that the prior art reference disclose each and every element of the claim to which it is applied. In re King, 801 F.2d, 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1996). Thus, there must be no differences between the subject matter of the claim and the disclosure of the prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: Absence from the applied reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

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Applicants respectfully submit that the claims of the present application are not anticipated by the disclosure of Wu since the applied reference does not disclose the claimed structure recited in amended Claim 1. Specifically, Wu does not disclose a semiconductor IC structure comprising: a semiconductor substrate including at least one front-end-of-the-line device (FEOL) located on a surface thereof; at least one *metal resistor* located on, or in close proximity to, said surface of said semiconductor substrate, said at least one metal resistor comprising at least a conductive metal; and *a first level of metallization above said at least one metal resistor*.

Wu provides a method of fabricating a semiconductor structure in which a salicide block mask comprising a lower buffer layer (440 or 640) such as a nitride etch stop layer and a dielectric layer (550) formed above the buffer layer. Applicants observe that in FIGS. 9 and 10 of Wu the labeling of the buffer layer and the dielectric layer is inconsistent with the previous drawings. In accordance with Wu, the salicide block mask is located atop a doped polysilicon region 430 that forms the resistor structure of the prior art. The doped polysilicon region 430 is located within the substrate in Wu.

Wu does not disclose a metal resistor as indicated by the Examiner. The layer referred to by the Examiner in the outstanding Office Action as the metal resistor was indicated to be element 600. The element 600 in Wu is not a metal resistor, but instead represents the blocking structure mentioned above.

Applicants further note that Wu does not disclose a first metallization level atop the metal resistor, as presently claimed. A metallization level, as is well known to those skilled in the art, represents a dielectric material that has conductive features (conductive vias and/or lines) embedded therein. Applicants find no such metallization level in Wu. Applicants note that the

Examiner referred to element 700 as the alleged first metallization level. Applicants respectfully disagree regarding this interpretation of element 700. In Wu, element 700 is a metal layer that is used in forming a silicide contact. The metal layer 700 that is not consumed during the silicidation process is removed and thus does not form a first metallization level.

The foregoing remarks clearly demonstrate that the applied reference does not teach each and every aspect of the claimed invention, as required by King and Kloster Speedsteel; therefore the claims of the present application are not anticipated by the disclosures of Wu. Applicants respectfully submit that the instant § 102 rejection has been obviated and withdrawal thereof is respectfully requested.

With respect to the various obviousness rejections, applicants submit the combined disclosures of Wu and Osanai et al. or Erdeljac et al. do not render the claimed structures obvious since the applied reference do not teach or suggest the structure presently claimed. That is, the combined disclosures of Wu and Osanai et al. or Erdeljac et al. do not teach or suggest a semiconductor IC structure comprising: a semiconductor substrate including at least one front-end-of-the-line device (FEOL) located on a surface thereof; at least one *metal resistor* located on, or in close proximity to, said surface of said semiconductor substrate, said at least one metal resistor comprising at least a conductive metal; and *a first level of metallization above said at least one metal resistor*.

The principal applied reference to Wu, which spurs each of the obviousness rejections, is defective for the reasons discussed above in regard to the anticipation rejection. Applicants thus incorporate the above remarks herein by reference. To reiterate: Wu discloses a silicide blocking structure that is located above a doped polysilicon region. The applied reference does not teach

or suggest a metal resistor, as presently claimed. Moreover, no metallization levels are taught or suggested in Wu.

The above defects in Wu are not alleviated by Osanai et al. and Erdeljak since the applied secondary references also do not teach or suggest the claimed structure in which a metal resistor is present and a first metallization level is located above the metal resistor. While Osanai et al. discloses metal resistor, it does not so in the context of including a first metallization level atop the metal resistor, as presently claimed. Erdeljak et al. is further removed that Osanai et al. since it is directed to polySi resistors, not metal resistors, as presently claimed.

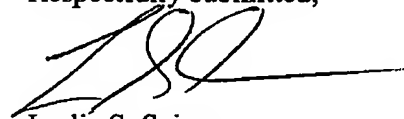
In view of the above remarks, the obviousness rejections citing Wu and Osanai et al. or Erdeljak et al. have been obviated. Reconsideration and withdrawal of the obviousness rejections are thus respectfully requested.

The various § 103 rejections also fail because there is no motivation in the applied references which suggest modifying the disclosed structures to include the various elements recited in the claims of the present invention. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejections under 35 U.S.C. § 103 have been obviated; therefore reconsideration and withdrawal thereof are respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



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